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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/852,819	05/09/2001	Jin H. Hwang	5440P001	5478

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EXAMINER	
PHAN, MAN U	

ART UNIT	PAPER NUMBER
2665	

DATE MAILED: 11/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/852,819	HWANG ET AL.	
	Examiner	Art Unit	
	Man Phan	2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 May 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-61* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,9,10,20-22,25-27 and 33-61* is/are rejected.

7)☒ Claim(s) *7,8,11-19,23,24 and 28-32* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02/20/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The application of Hwang et al. for a "Method and apparatus for aligning multiple data streams and matching transmission rates of multiple data" filed 05/09/2001 has been examined. Claims 1-61 are pending in the application.

Claim Rejections - 35 USC ' 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by prior art under 35 U.S.C. 103(a).

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 1038 and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 33-61 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pfahler et al. (US#6,771,670) in view of Koyanagi et al. (US#6,636,993).

With respect to claims 43-50, Pfahler and Koyanagi disclose a time alignment apparatus for receiving successive data frames on a plurality of channels with respect to a common synchronization clock, according to the essential features of the claims. Pfahler teaches in Fig. 1 a block circuit diagram illustrated a time alignment apparatus of a receiver for aligning communication channels, comprising: at least a first, second and third read/write frame memory for respectively storing one data frame of each of said channels, said frame memories each having a write state in which data is written to said frame memories and a read state in which data is read from said frame memories; and a control unit for cyclically switching said three frame memories through a first to third alignment mode synchronized to said common synchronization clock, wherein after each mode switching a newly arriving data frame of any channel is always written to a frame memory which was in a read state in the previous mode; and wherein data frames are always read from the frame memory having a read state time-aligned to said common synchronization clock (Col. 2; lines 13 plus).

However, Pfahler does not expressly disclose a control code detector to detect aligning codes, monitor the occurrence of aligning codes. In the same field of endeavor, Koyanagi et al. teaches a system and method for performing automatic deskew tuning and alignment across high-speed, parallel interconnections in a high performance digital system to compensate for inter-bit skew. Koyanagi discloses in Fig. 1 is a block diagram of an automatic deskew system 100 for use in high-speed, parallel interconnections for digital systems in accordance with one

embodiment of the present invention. The digital system may be, for example, a high performance microprocessor, memory system or router chip. The automatic deskew system 100 includes a plurality of deskew subsystems 192 and 180, and a deskew controller 135. One deskew subsystem resides at the receiving end of each parallel interconnection. In accordance with the present invention, the automatic deskew system has at least two deskew subsystems, but the precise number of such deskew subsystems varies depending upon the number of parallel interconnections in the digital system. A deskew subsystem has a single bit input 145a which receives a skewed signal and a four bit output 160a-160d, and is coupled to the deskew controller 135. The signal on input 145a carries one bit of information every one bit time, T. "One bit time" or "T" is defined as 1/N seconds where N is the number of bits of information transmitted on an interconnection in one second. The signals on the four bit output 160a-160d are corrected for skew and unfolded. In other words, each output is properly aligned with the other output signals and the rate of each output has been reduced by a factor of four relative to the input 145a (Col, 3, lines 52 plus). Koyanagi further teaches in Fig. 10A a functional block diagram illustrated the deskew controller 135. The deskew controller 135 includes a selector 1000, a controller 1035, four detectors 1015, 1020, 1025 and 1030, and a plurality of registers 1050 and 1055, the number of registers depends upon the number of parallel interconnections. Detectors 1025 and 1030 receive inputs directly from the outputs of each deskew subsystem, e.g., 192 and 180, in the digital system. Detector 1025 detects for all "1" values, and detector 1030 detects for all "0" values. The outputs 1080a and 1080b of detectors 1025 and 1030, respectively, are input into the controller 1035 so that the controller 1035 can compute the delays between or among each parallel input interconnection 145a and 145b in the digital system (Col. 6, lines 25 plus).

Regarding claims 51-61, they are method claims corresponding to the apparatus claims 43-50 above. Therefore, claims 51-56 are analyzed and rejected as previously discussed in paragraph above with respect to claims 43-50.

Regarding claims 33-42, they are system claims corresponding to the method and apparatus claims above. Therefore, claims 33-42 are analyzed and rejected as previously discussed in paragraph above with respect to claims 43-61 above.

One skilled in the art would have recognized the need for effectively and efficiently controlling the data transmission rates utizing time-aligning data frames of a plurality of channels, and would have applied Koyanagi's novel use of the automatic deskew tuning and alignment across high speed, parallel interconnections into Pfahler's teaching of the time alignment for receiving successive data frames on a plurality of channels. Therefore, It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to apply Koyanagi's system and method for automatic deskew across a high speed, parallel interconnections into Pfahler's time-alignment apparatus and method for time-aligning data frames of a plurality of channels in a telecommunication systemwith the motivation being to provide a method and system for aligning multiple data channels with one receiving rate.

5. Claims 1-6, 9-10 and 20-22, 25-27are rejected under 35 U.S.C. 103(a) as being unpatentable over Pfahler et al. (US#6,771,670) in view of Koyanagi et al. (US#6,636,993) as applied to the claims above, and further in view of Jin et al. (US#6,173,380).

With respect to claims 1-6, 9-10, Pfahler et al. and Koyanagi et al. disclose the claimed limitations discussed in paragraph 4 above. However, Pfahler et al. and Koyanagi et al. do not

expressly disclose the process of holding the aligning character and subsequently received input characters for each input channel in the corresponding buffer until an aligning character has been detected on every input channel. In the same field of endeavor, Jin et al. teaches an apparatus and method for aligning any number of multiple parallel channels of data signals according to a single clock is provided. The synchronization process is accomplished through the use of a First-In-First-Out (FIFO) principle and individual storage elements implementing the FIFO principle for each received data channel. Each channel's data signals are read into a corresponding storage element, maintained in order, and read out upon the assertion of read signals in synchronization with a designated single clock signal. The apparatus and method preferably uses indications of data ready to be read from a storage element implementing the FIFO principle and the presence of a master clock signal to activate the reading of the data from the corresponding storage element. Therefore, each data channel is fully aligned with the master clock signal. The alignment function is based on a FIFO principle. Clock-data signal pairs arrive at the device with random and unknown delays between them. Each signal pair data stream is written into an individual storage element. After allowing data to be written in, the storage element will receive a read assertion signal, allowing the stored data signals to be read out in conjunction with the master clock signal--achieving full synchronization with the master clock signal (Col. 3, lines 42 plus).

Regarding claims 20-22, 25-27, they are method claims corresponding to the apparatus claims 1-6, 9-10 above. Therefore, claims 20-22, 25-27 are analyzed and rejected as previously discussed in paragraph above with respect to claims 1-6, 9-10.

One skilled in the art would have recognized the need for effectively and efficiently controlling the data transmission rates utizing time-aligning data frames of a plurality of channels, and would have applied Jin's multiple receive clock data channel alignment device ans Koyanagi's novel use of the automatic deskew tuning and alignment across high speed, parallel interconnections into Pfahler's teaching of the time alignment for receiving successive data frames on a plurality of channels. Therefore, It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to apply Jin's apparatus and method for providing multiple channel clock data alignment, and Koyanagi's system and method for automatic deskew across a high speed, parallel interconnections into Pfahler's time-alignment apparatus and method for time-aligning data frames of a plurality of channels in a telecommunication systemwith the motivation being to provide a method and system for aligning multiple data channels with one receiving rate.

Allowable Subject Matter

6. Claims 7-8, 11-19 and 23-24, 28-32 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is an examiner's statement of reasons for the indication of allowable subject matter: The closest prior art of record fails to disclose or suggest wherein the control unit to stop holding the aligning character and subsequently received input characters for each input channel

in the corresponding buffer if an aligning character has not been detected on every input channel within a given period of time/characters from the first detected aligning character, as recited in the claims.

8. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The Walker et al. (US#6,650,638) is cited to show the decoding method and decoder for 64B/66B coded pactketized serial data.

The Niegel (US#5,802,122) is cited to show the transmission system comprising a matching circuit.

The Godbole (US#6,606,775) is cited to show the clock synchronization in systems with multi-channel high speed bus subsystems.

The Little (US#5,461,621) is cited to show the pair division multiplexer for digital communications.

The Miki et al. (US#6,738,393) is cited to show the frame synchronization circuit.

The Park et al. (US#6,397,367) is cited to show the device and methods for channel coding and rate matching in a communication system.

The Mundkur et al. (US#2002/0122435) is cited to show the scalable multi-channel frame aligner.

The Teng (US#2003/0031202) is cited to show the aligning data packets/frames for transmission over a network channel.

10. Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703)308-9051, (for formal communications intended for entry)

or:

(703)308-5399, (for informal or draft communications, please label "PROPOSED" or "DRAFT"

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystals Drive, Arlington, VA., Sixth Floor (Receptionist).

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to M. Phan whose telephone number is (571) 272-3149.

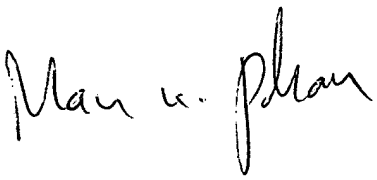
The examiner can normally be reached on Mon - Fri from 6:30 to 3:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu, can be reached on (571) 272-3155. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-2600.

MPhan

11/05/2004



MAN U. PHAN
PRIMARY EXAMINER